National Semiconductor

December 18, 2007

LMP2015 Single/LMP2016 Dual High Precision, Rail-to-Rail Output Operational Amplifier

General Description

The LMP2015/LMP2016 are the first members of National's new LMP™ precision amplifier family. The LMP2015/LMP2016 offer unprecedented accuracy and stability in space-saving miniature packaging at an affordable price. These devices utilize patented techniques to measure and continually correct the input offset error voltage. The result is a series of amplifiers which are ultra stable over time and temperature. They have excellent CMRR and PSRR ratings, and do not exhibit the familiar 1/f voltage and current noise increase that plagues traditional amplifiers. The combination of characteristics makes the LMP2015/LMP2016 good choices for transducer amplifiers, high gain configurations, ADC buffer amplifiers, DAC I-V conversion, or any other 2.7V-5V application requiring precision and long term stability.

Other useful benefits of the LMP2015/LMP2016 are rail-to-rail output, a low supply current of 930 µA, and a wide gain bandwidth product of 3 MHz. These extremely versatile features provide high performance and ease of use.

Features

(For V_S = 5V, Typical unless otherwise noted)

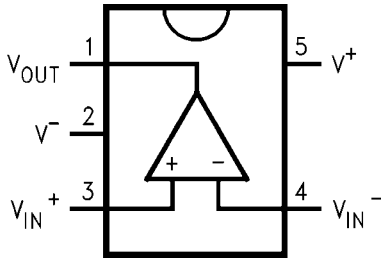
- Low guaranteed V_{OS} over temperature — 10 µV
- Low noise with no 1/f — 35 nV/√Hz
- High CMRR — 130 dB
- High PSRR — 120 dB
- High A_{VOL} — 130 dB
- Wide gain bandwidth product — 3 MHz
- High slew rate — 4 V/µs
- Low supply current — 930 µA
- Rail-to-Rail output — 30 mV
- No external capacitors required

Applications

- Precision instrumentation amplifiers
- Thermocouple amplifiers
- Strain gauge bridge amplifier
- ADC driver

Connection Diagrams

5-Pin SOT23



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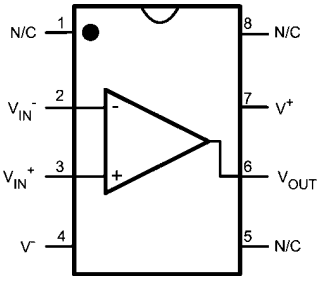
Top View

8-Pin SOIC



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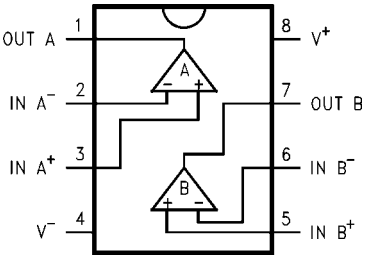
Top View

8-Pin MSOP



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Top View

Ordering Information

Package	Part Number	Temperature Range	Package Marking	Transport Media	NSC Drawing
5-Pin SOT23	LMP2015MF	−40°C to 125°C	AD5A	1k Units Tape and Reel	MF05A
	LMP2015MFX			3k Units Tape and Reel	
8-Pin SOIC	LMP2015MA		LMP2015MA	95 Units/Rail	M08A
	LMP2015MAX			2.5k Units Tape and Reel	
	LMP2016MA		LMP2016MA	95 Units/Rail	
	LMP2016MAX			2.5k Units Tape and Reel	
8-Pin MSOP	LMP2016MM		AE5A	1k Units Tape and Reel	MUA08A
	LMP2016MMX			3.5k Units Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	2000V
Machine Model	200V
Supply Voltage	5.8V
Common Mode Input Voltage	$-0.3 \le V_{CM} \le V_{CC} +0.3V$
Lead Temperature (soldering 10 sec.)	+300°C
Differential Input Voltage	±Supply Voltage
Current at Input Pin	30 mA
Current at Output Pin	30 mA
Current at Power Supply Pin	50 mA

Operating Ratings (Note 1)

Supply Voltage	2.7V to 5.25V
Storage Temperature Range	−65°C to 150°C
Temperature Range (Note 3)	−40°C to 125°C

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.35V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{OS}	Input Offset Voltage (LMP2015 only)			0.8	5 **10**	µV
	Input Offset Voltage (LMP2016 only)			0.8	5 **10**	µV
	Offset Calibration Time			0.5	10 **12**	ms
TCV_{OS}	Input Offset Voltage			0.015	.05	µV/°C
	Long Term Offset Drift			0.006		µV/month
	Lifetime V_{OS} Drift			2.5		µV
I_{IN}	Input Current			-3		pA
I_{OS}	Input Offset Current			6		pA
R_{IND}	Input Differential Resistance			9		MΩ
CMRR	Common Mode Rejection Ratio	$-0.3 \le V_{CM} \le 0.9V$ $0 \le V_{CM} \le 0.9V$	95 **90**	130		dB
CMVR	Input Common Mode Range	CMRR ≥ 95 dB	−0.3		0.9	dB
		CMRR ≥ 90 dB	0		0.9	dB
PSRR	Power Supply Rejection Ratio	$V^+ - V^-$ = 2.7V to 5V, V_{CM} = 0V	95 **90**	120		dB
V_O	Output Swing (LMP2015 only)	R_L = 10 kΩ to 1.35V V_{IN}(diff) = ±0.5V	2.665 **2.655**	2.68		V
				0.033	0.060 **0.075**	V
		R_L = 2 kΩ to 1.35V V_{IN}(diff) = ±0.5V	2.630 **2.615**	2.65		V
				0.061	0.085 **0.105**	V
	Output Swing (LMP2016 only)	R_L = 10 kΩ to 1.35V V_{IN}(diff) = ±0.5V	2.64 **2.63**	2.68		V
				0.033	0.060 **0.075**	V
		R_L = 2 kΩ to 1.35V V_{IN}(diff) = ±0.5V	2.615 **2.6**	2.65		V
				0.061	0.085 **0.105**	V

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
A_{VOL}	Open Loop Voltage Gain	R_L = 10 kΩ	95 **90**	130		dB
		R_L = 2 kΩ	90 **85**	124		
I_O	Output Current	Sourcing, V_O = 0V V_{IN}(diff) = ±0.5V	5 **3**	12		mA
		Sinking, V_O = 5V V_{IN}(diff) = ±0.5V	5 **3**	18		
I_S	Supply Current per Channel			0.919	1.20 **1.50**	mA

2.7V AC Electrical Characteristics

T_A = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.35V, V_O = 1.35V, and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
GBWP	Gain Bandwidth Product			3		MHz
SR	Slew Rate			4		V/µs
θ_m	Phase Margin			60		Deg
G_m	Gain Margin			–14		dB
e_n	Input Referred Voltage Noise			35		$nV/\sqrt{Hz}$
i_n	Input Referred Current Noise					$pA/\sqrt{Hz}$
e_np-p	Input Referred Voltage Noise	R_S = 100Ω, DC to 10 Hz		850		nV_{PP}
t_{rec}	Input Overload Recovery Time			50		ms

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_O = 2.5V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{OS}	Input Offset Voltage (LMP2015 only)			0.12	5 **10**	µV
	Input Offset Voltage (LMP2016 only)			0.12	5 **10**	
	Offset Calibration Time			0.5	10 **12**	ms
TCV_{OS}	Input Offset Voltage			0.015	.05	µV/°C
	Long Term Offset Drift			0.006		µV/month
	Lifetime V_{OS} Drift			2.5		µV
I_{IN}	Input Current			–3		pA
I_{OS}	Input Offset Current			6		pA
R_{IND}	Input Differential Resistance			9		MΩ
CMRR	Common Mode Rejection Ratio	$-0.3 \le V_{CM} \le 3.2$ $0 \le V_{CM} \le 3.2$	100 **90**	130		dB
CMVR	Input Common Mode Range	CMRR ≥ 100 dB	–0.3		3.2	dB
		CMRR ≥ 90 dB	0		3.2	
PSRR	Power Supply Rejection Ratio	$V^+ - V^-$ = 2.7V to 5V, V_{CM} = 0V	95 **90**	120		dB

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_O	Output Swing (LMP2015 only)	R_L = 10 kΩ to 2.5V V_{IN}(diff) = ±0.5V	4.96 **4.95**	4.978		V
				0.040	0.070 **0.085**	
		R_L = 2 kΩ to 2.5V V_{IN}(diff) = ±0.5V	4.895 **4.875**	4.919		V
				0.091	0.115 **0.140**	
	Output Swing (LMP2016 only)	R_L = 10 kΩ to 2.5V V_{IN}(diff) = ±0.5V	4.92 **4.91**	4.978		V
				0.040	0.080 **0.095**	
		R_L = 2 kΩ to 2.5V V_{IN}(diff) = ±0.5V	4.875 **4.855**	4.919		V
				0.0.91	0.125 **0.150**	
A_{VOL}	Open Loop Voltage Gain	R_L = 10 kΩ	105 **100**	130		dB
		R_L = 2 kΩ	95 **90**	132		
I_O	Output Current	Sourcing, V_O = 0V V_{IN}(diff) = ±0.5V	8 **6**	15		mA
		Sinking, V_O = 5V V_{IN}(diff) = ±0.5V	8 **6**	17		
I_S	Supply Current per Channel			0.930	1.20 **1.50**	mA

5V AC Electrical Characteristics

T_A = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_O = 2.5V, and R_L > 1 MΩ.
Boldface limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
GBW	Gain-Bandwidth Product			3		MHz
SR	Slew Rate			4		V/µs
θ_m	Phase Margin			60		deg
G_m	Gain Margin			−15		dB
e_n	Input-Referred Voltage Noise			35		$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise					$pA/\sqrt{Hz}$
e_np-p	Input-Referred Voltage Noise	R_S = 100Ω, DC to 10 Hz		850		nV_{PP}
t_{rec}	Input Overload Recovery Time			50		ms

Note 1: Absolute Maximum Ratings indicate limits beyond which damage may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)

Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

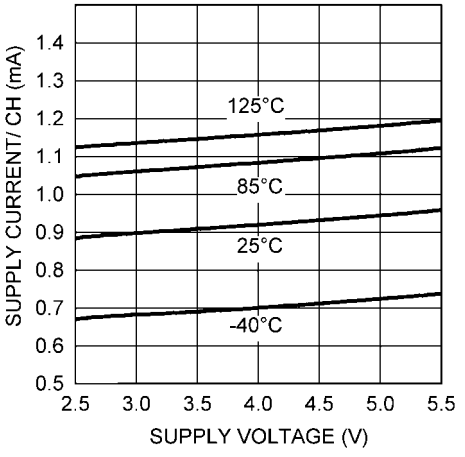
Note 4: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 5: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using statistical quality control (SQC) method.

Typical Performance Characteristics

T_A = 25°C, V_S = 5V unless otherwise specified.

Supply Current vs. Supply Voltage



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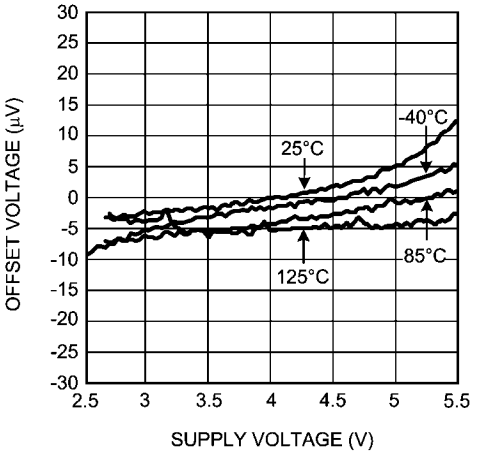
Offset Voltage vs. Supply Voltage



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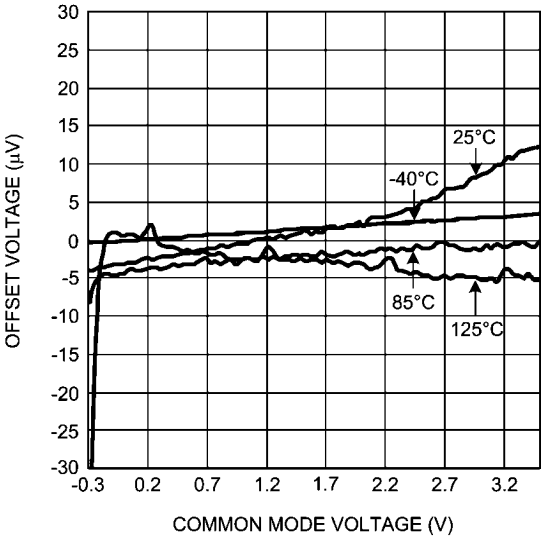
Offset Voltage vs. Common Mode Voltage (V_S = +5V)



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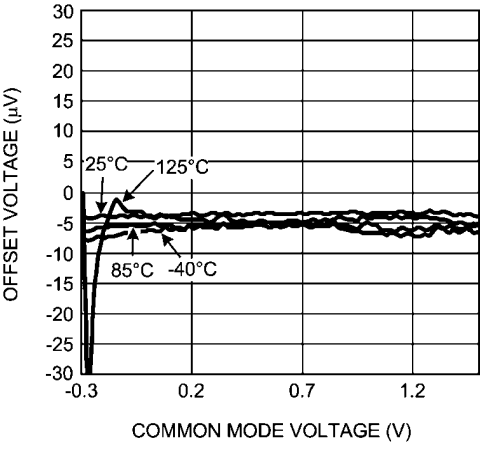
Offset Voltage vs. Common Mode Voltage (V_S = +2.7V)



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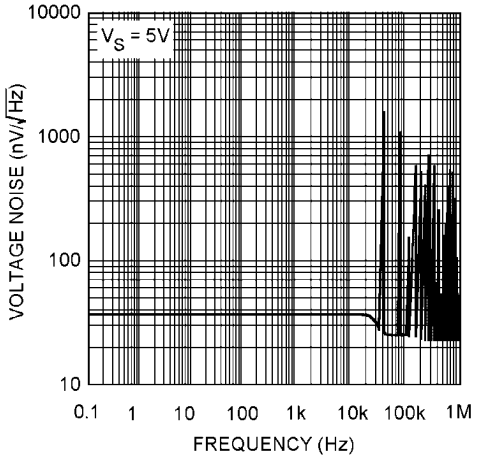
Voltage Noise vs. Frequency



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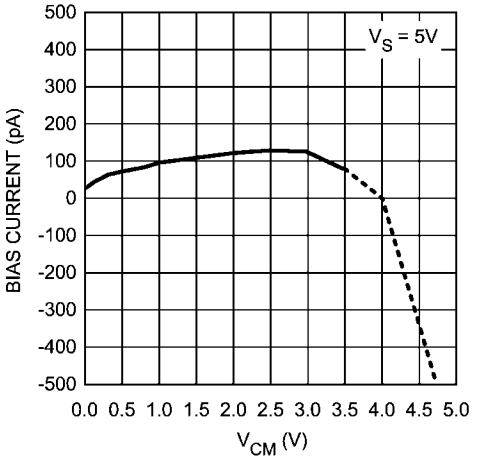
Input Bias Current vs. Common Mode



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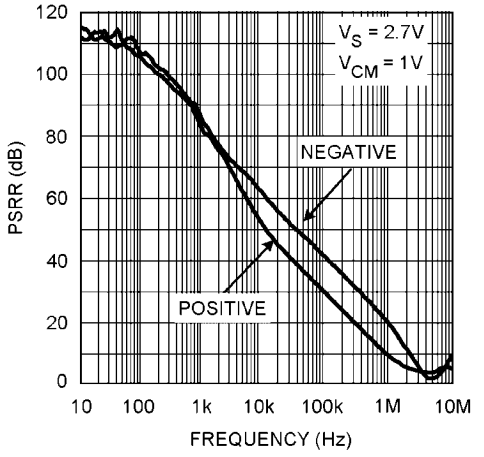
PSRR vs. Frequency



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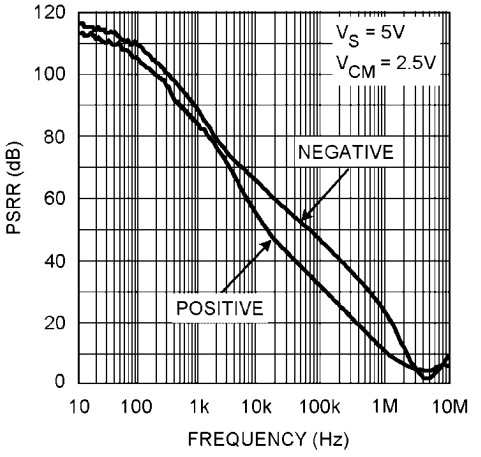
PSRR vs. Frequency



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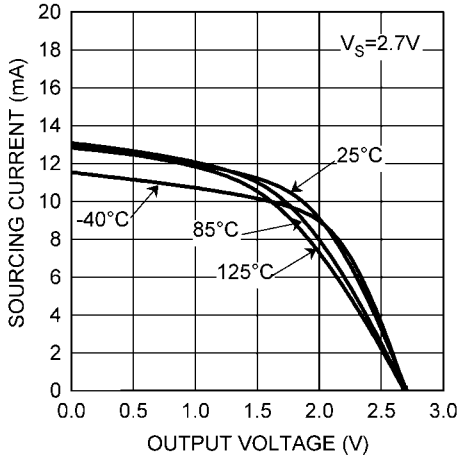
Output Sourcing @ 2.7V



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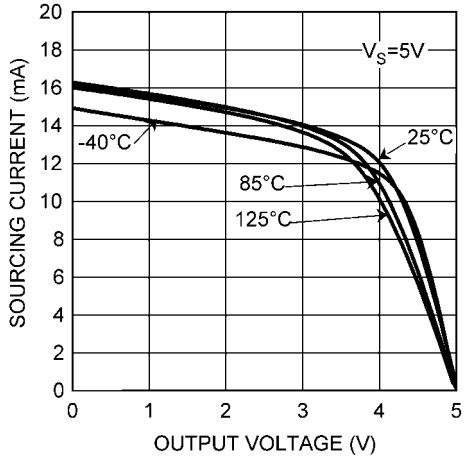
Output Sourcing @ 5V



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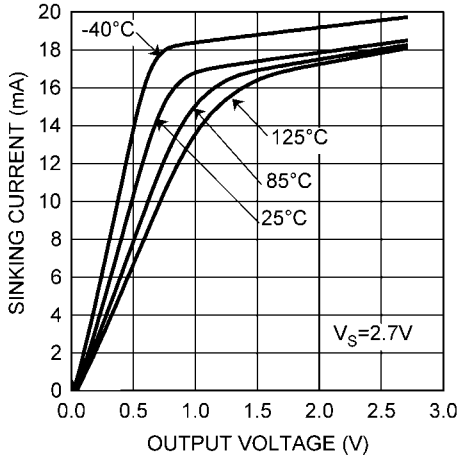
Output Sinking @ 2.7V



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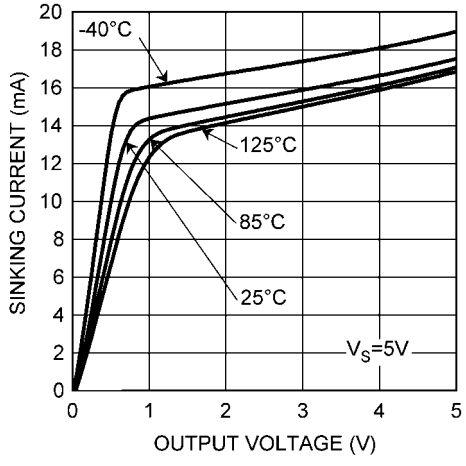
Output Sinking @ 5V



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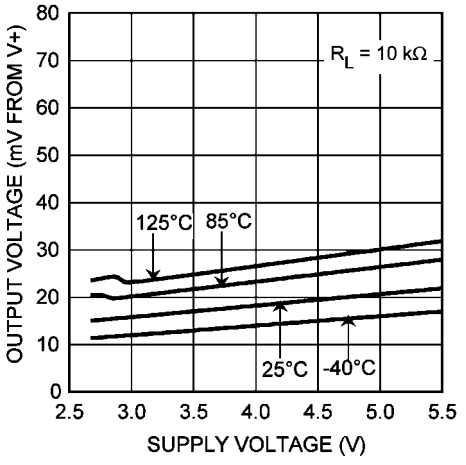
Maximum Output Swing vs. Supply Voltage



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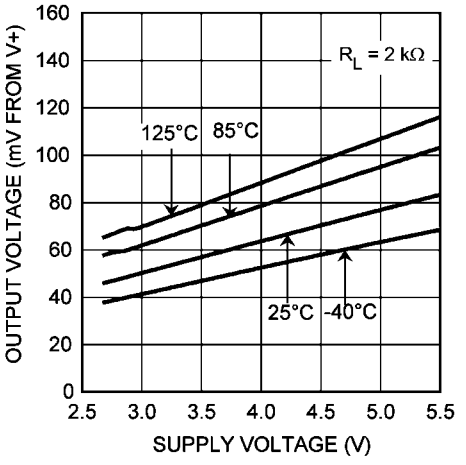
Maximum Output Swing vs. Supply Voltage



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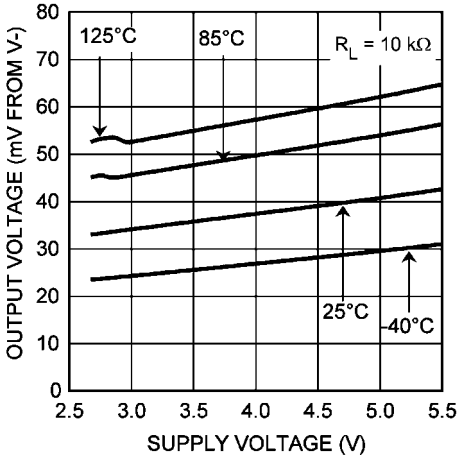
Minimum Output Swing vs. Supply Voltage



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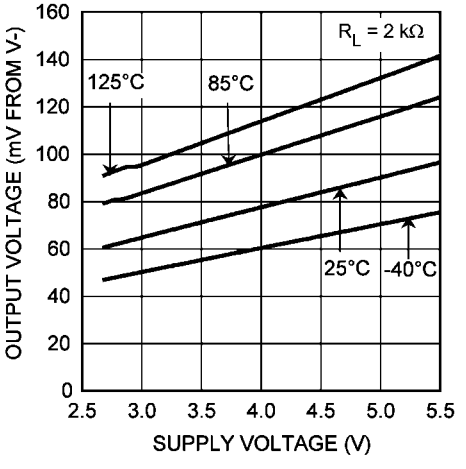
Minimum Output Swing vs. Supply Voltage



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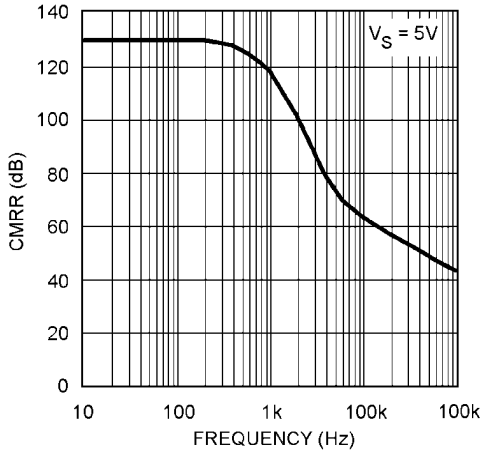
CMRR vs. Frequency



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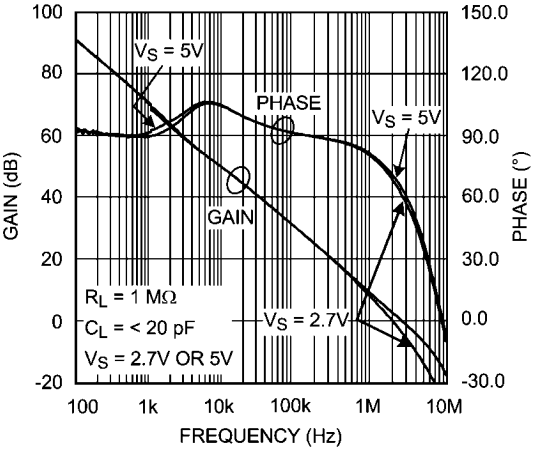
Open Loop Gain and Phase vs. Supply Voltage



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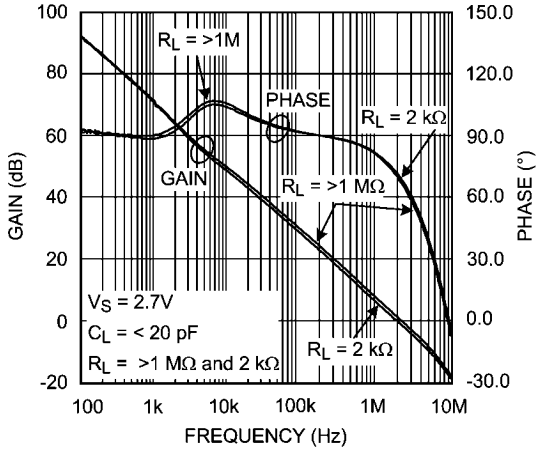
Open Loop Gain and Phase vs. Resistive Load @ 2.7V



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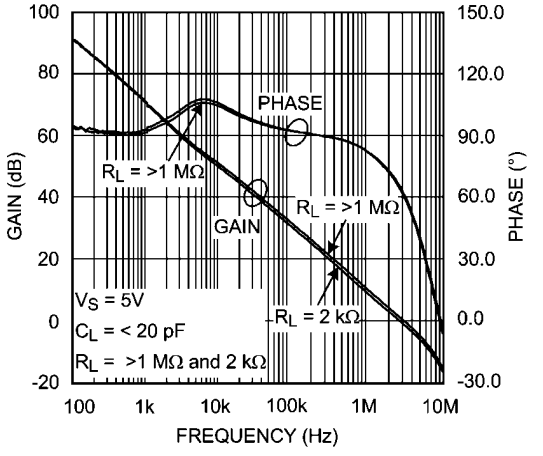
Open Loop Gain and Phase vs. Resistive Load @ 5V



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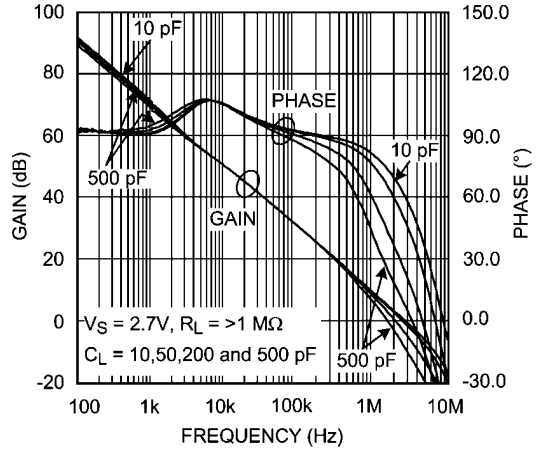
Open Loop Gain and Phase vs. Capacitive Load @ 2.7V



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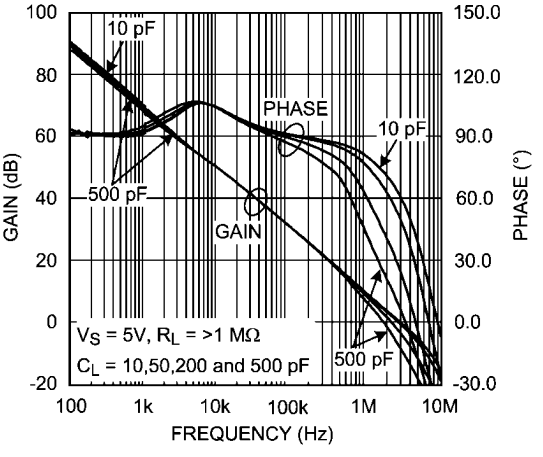
Open Loop Gain and Phase vs. Capacitive Load @ 5V



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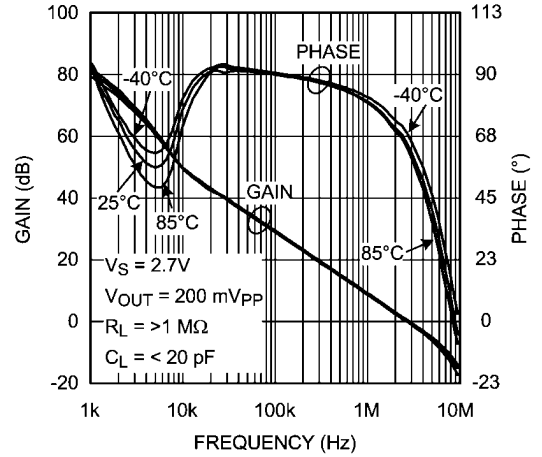
Open Loop Gain and Phase vs. Temperature @ 2.7V



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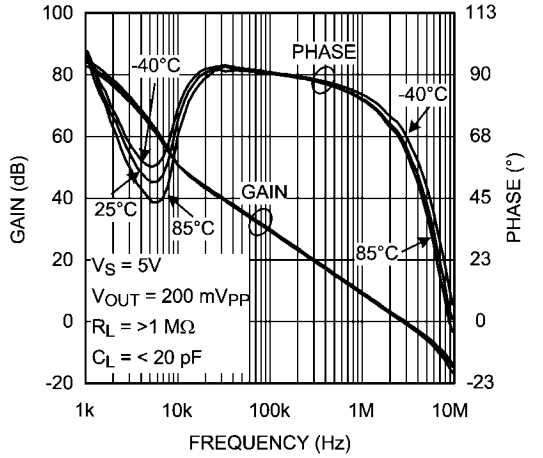
Open Loop Gain and Phase vs. Temperature @ 5V



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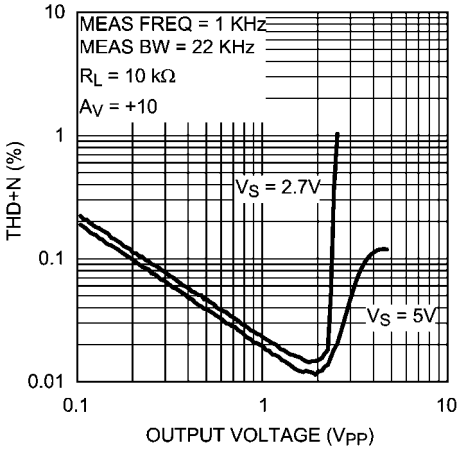
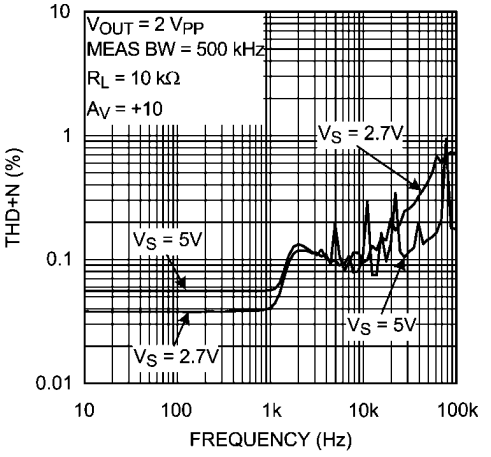
THD+N vs. Amplitude



20212514

THD+N vs. Frequency



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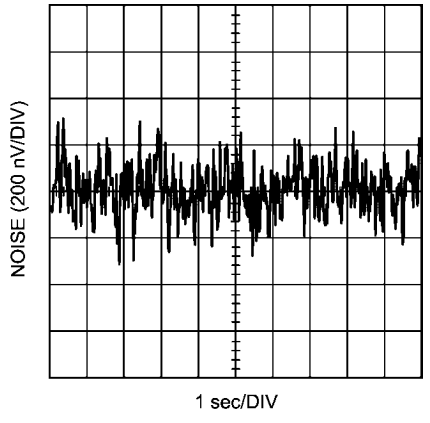
0.1 Hz – 10 Hz Noise vs. Time



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Application Information

THE BENEFITS OF THE LMP2015/LMP2016's NO 1/f NOISE

Using patented methods, the LMP2015/LMP2016 eliminate the 1/f noise present in other amplifiers. That noise, which increases as frequency decreases, is a major source of measurement error in all DC-coupled measurements. Low frequency noise appears as a constantly changing signal in series with any measurement being made. As a result, even when the measurement is made rapidly, this constantly changing noise signal will corrupt the result. The value of this noise signal can be surprisingly large. For example: If a conventional amplifier has a flat-band noise level of 10 nV/$\sqrt{\text{Hz}}$ and a noise corner of 10 Hz, the RMS noise at 0.001 Hz is 1 μV/$\sqrt{\text{Hz}}$. This is equivalent to a 0.50 μV peak-to-peak error, in the frequency range 0.001 Hz to 1.0 Hz. In a circuit with a gain of 1000, this produces a 0.50 mV peak-to-peak output error. This number of 0.001 Hz might appear unreasonably low, but when a data acquisition system is operating for 17 minutes, it has been on long enough to include this error. In this same time, the LMP2015/LMP2016 will have only a 0.21 mV output error. This is smaller by 2.4 x. Keep in mind that this 1/f error gets even larger at lower frequencies. At the extreme, many people try to reduce this error by integrating or taking several samples of the same signal. This is also doomed to failure because the 1/f nature of this noise means that taking longer samples just moves the measurement into lower frequencies where the noise level is even higher.

The LMP2015/LMP2016 eliminate this source of error. The noise level is constant with frequency so that reducing the bandwidth reduces the errors caused by noise.

Another source of error that is rarely mentioned is the error voltage caused by the inadvertent thermocouples created when the common "Kovar type" IC package lead materials are soldered to a copper printed circuit board. These steel based leadframe materials can produce over 35 μV/°C when soldered onto a copper trace. This can result in thermocouple noise that is equal to the LMP2015/LMP2016 noise when there is a temperature difference of only 0.0014°C between the lead and the board!

For this reason, the lead frame of the LMP2015/LMP2016 is made of copper. This results in equal and opposite junctions which cancel this effect. The extremely small size of the SOT23 package results in the leads being very close together. This further reduces the probability of temperature differences and hence decreases thermal noise.

OVERLOAD RECOVERY

The LMP2015/LMP2016 recover from input overload much faster than most chopper-stabilized op amps. Recovery from driving the amplifier to 2X the full scale output, only requires about 40 ms. Many chopper-stabilized amplifiers will take from 250 ms to several seconds to recover from this same overload. This is because large capacitors are used to store the unadjusted offset voltage.

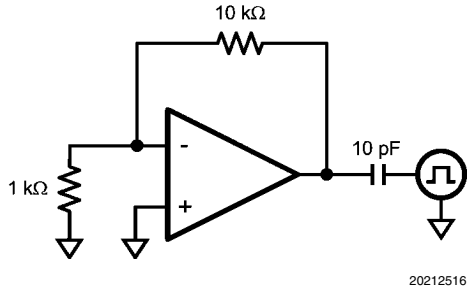


FIGURE 1. Overload Recovery Test

The wide bandwidth of the LMP2015/LMP2016 enhance performance when it is used as an amplifier to drive loads that inject transients back into the output. ADCs (Analog-to-Digital Converters) and multiplexers are examples of this type of load. To simulate this type of load, a pulse generator producing a 1V peak square wave was connected to the output through a 10 pF capacitor. (*Figure 1*) The typical time for the output to recover to 1% of the applied pulse is 80 ns. To recover to 0.1% requires 860 ns. This rapid recovery is due to the wide bandwidth of the output stage and large total GBWP.

NO EXTERNAL CAPACITORS REQUIRED

The LMP2015/LMP2016 do not need external capacitors. This eliminates the problems caused by capacitor leakage and dielectric absorption, which can cause delays of several seconds from turn-on until the amplifier's error has settled.

MORE BENEFITS

The LMP2015/LMP2016 offer the benefits mentioned above and more. These parts have rail-to-rail outputs and consume only 950 μA of supply current while providing excellent DC and AC electrical performance. In DC performance, the LMP2015/LMP2016 achieve 130 dB of CMRR, 120 dB of PSRR and 130 dB of open loop gain. In AC performance, the LMP2015/LMP2016 provide 3 MHz of gain bandwidth product and 4 V/μs of slew rate.

HOW THE LMP2015/LMP2016 WORK

The LMP2015/LMP2016 use new, patented techniques to achieve the high DC accuracy traditionally associated with chopper-stabilized amplifiers without the major drawbacks produced by chopping. The LMP2015/LMP2016 continuously monitor the input offset and correct this error. The conventional chopping process produces many mixing products, both sums and differences, between the chopping frequency and the incoming signal frequency. This mixing causes a large amount of distortion, particularly when the signal frequency approaches the chopping frequency. Even without an incoming signal, the chopper harmonics mix with each other to produce even more trash. To explain this *Figure 2* shows a plot, of the output of a typical (MAX432) chopper-stabilized op amp. This is the output when there is no incoming signal, just the amplifier in a gain of –10 with the input grounded. The chopper is operating at about 150 Hz; the rest is mixing products. Add an input signal and the noise gets much worse. Compare this plot with *Figure 3* of the LMP2015/LMP2016. This data was taken under the exact same conditions. The auto-zero action is visible at about 30 kHz but note the absence of mixing products at other frequencies. As a result, the LMP2015/LMP2016 have very low distortion of 0.02% and very low mixing products.

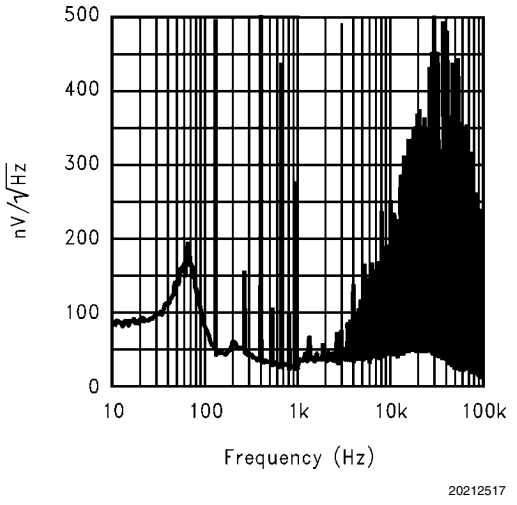


FIGURE 2. The Output of a Chopper Stabilized Op Amp (MAX432)

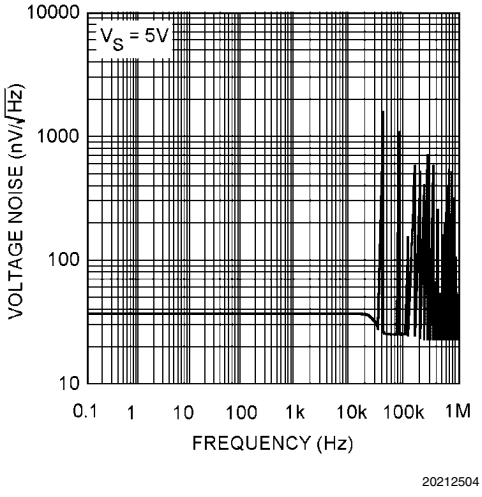


FIGURE 3. The Output of the LMP2015/LMP2016

INPUT CURRENTS

The LMP2015/LMP2016 input currents are different than standard bipolar or CMOS input currents in that it appears as a current flowing in one input and out the other. Under most operating conditions, these currents are in the picoamp level and will have little or no effect in most circuits. These currents tend to increase slightly when the common-mode voltage is near the minus supply. (See the typical curves.) At high temperatures such as 85°C, the input currents become larger, 0.5 nA typical, and are both positive except when the V_{CM} is near V^-. If operation is expected at low common-mode voltages and high temperature, do not add resistance in series with the inputs to balance the impedances. Doing this can cause an increase in offset voltage. A small resistance such as 1 kΩ can provide some protection against very large transients or overloads, and will not increase the offset significantly.

PRECISION STRAIN GAUGE AMPLIFIER

This strain gauge amplifier (*Figure 4*) provides high gain (1006 or ~60 dB) with very low offset and drift. Using the resistors' tolerances as shown, the worst case CMRR will be greater than 108 dB. The CMRR is directly related to the resistor mismatch. The rejection of common-mode error, at the output, is independent of the differential gain, which is set by R3. The CMRR is further improved, if the resistor ratio matching is improved, by specifying tighter-tolerance resistors, or by trimming.

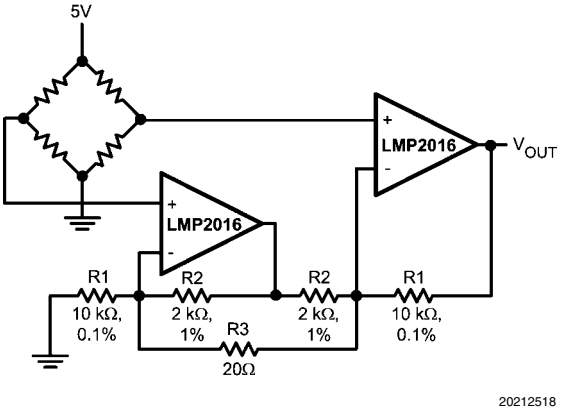


FIGURE 4. Precision Strain Gauge Amplifier

Extending Supply Voltages and Output Swing by Using a Composite Amplifier Configuration

In cases where substantially higher output swing is required with higher supply voltages, arrangements such as those shown in *Figure 5* and *Figure 6* can be used. These configurations utilize the excellent DC performance of the LMP2015 while allowing the superior voltage and frequency capabilities of the LM6171 to set the dynamic performance of the overall amplifier. For example, it is possible to achieve ±12V output swing with 300 MHz of overall GBW (A_V = 100) while keeping the worst case output shift due to V_{OS} less than 4 mV. The LMP2015 output voltage is kept at about mid-point of its overall supply voltage, and its input common mode voltage range allows the V^- terminal to be grounded in one case (*Figure 5*, inverting operation) and tied to a small non-critical negative bias in another (*Figure 6*, non-inverting operation). Higher closed loop gains are also possible with a corresponding reduction in realizable bandwidth. Table 1 shows some other closed loop gain possibilities along with the measured performance in each case.

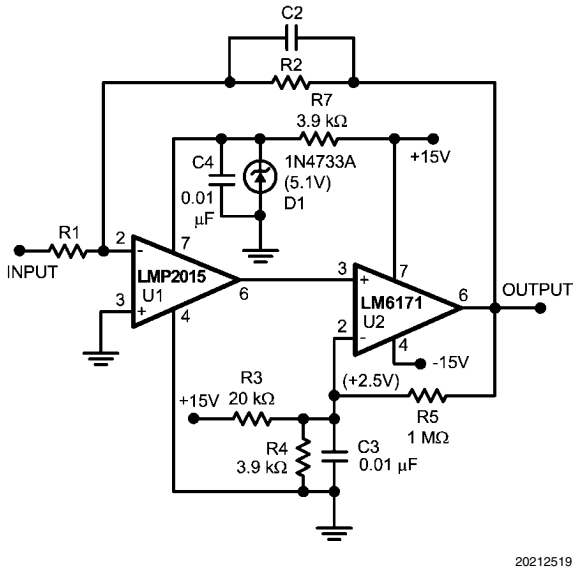


FIGURE 5. Composite Amplifier Configuration

TABLE 1. Composite Amplifier Measured Performance

AV	R1 Ω	R2 Ω	C2 pF	BW MHz	SR (V/µs)	en p-p (mV_{PP})
50	200	10k	8	3.3	178	37
100	100	10k	10	2.5	174	70
100	1k	100k	0.67	3.1	170	70
500	200	100k	1.75	1.4	96	250
1000	100	100k	2.2	0.98	64	400

In terms of the measured output peak-to-peak noise, the following relationship holds between output noise voltage; e_n p-p, the closed-loop gain; A_V, and –3 dB bandwidth; BW:

$$\frac{e_{npp1}}{e_{npp2}} = \sqrt{\frac{BW1}{BW2}} \bullet \frac{A_V1}{A_V2} \quad (1)$$

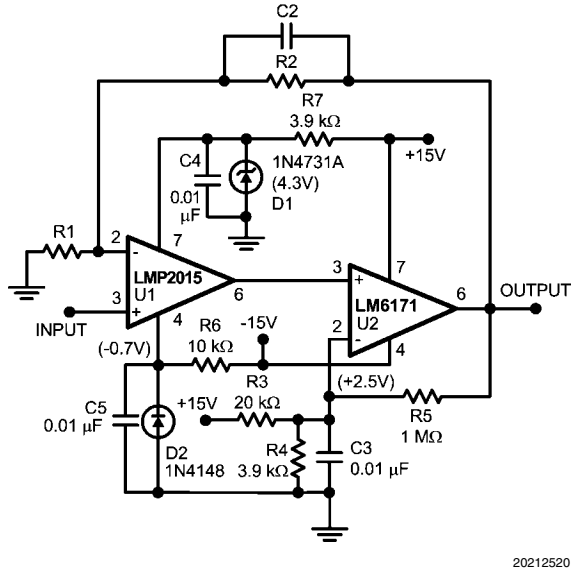


FIGURE 6. Composite Amplifier Configuration

It should be kept in mind that in order to minimize the output noise voltage for a given closed loop gain setting, one could minimize the overall bandwidth. As can be seen from *Equation 1*, the output noise has a square root relationship to the bandwidth.

In the case of the inverting configuration, it is also possible to increase the input impedance of the overall amplifier by raising the value of R1. This can be done without having to increase the feedback resistor, R2, to impractical values, by utilizing a "Tee" network as feedback. See the LMC6442 datasheet (Application Information section) for more details on this.

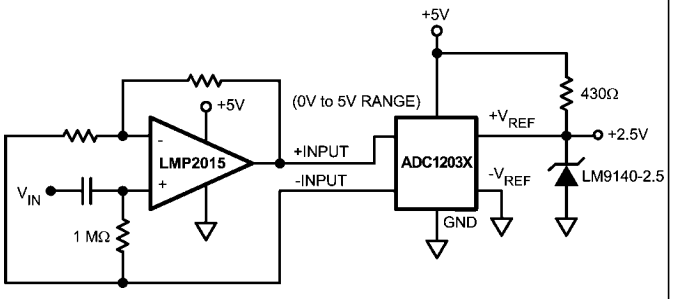


FIGURE 7. AC Coupled ADC Driver

LMP2015 AS AN ADC DRIVER

The LMP2015 is a great choice for an amplifier stage immediately before the input of an ADC (Analog-to-Digital Converter) as an ADC driver, whether AC or DC coupled. See *Figure 7* and *Figure 8*. This is because of the following important characteristics:

A) Very low offset voltage and offset voltage drift over time and temperature allow a high closed loop gain setting without introducing any short term or long term errors. For example, when set to a closed loop gain of 100 as the analog input amplifier for a 12-bit A/D converter, the overall conversion error over full operation temperature and 30 year life of the part (operating at 50°C) would be less than 5 LSBs.

B) Fast large signal settling time to 0.01% of final value (1.4 µs) allows 12-bit accuracy at a sampling rate of 100 kHz or more.

C) No flicker (1/f) noise means unsurpassed data accuracy over any measurement period of time, no matter how long. Consider the following op amp performance, based on a typical low noise, high performance commercially-available device, for comparison:

Op amp flatband noise = 8 $nV/\sqrt{Hz}$

1/f corner frequency = 100 Hz

A_V = 2000

Measurement time = 100 sec

Bandwidth = 2 Hz

This example will result in about 2.2 mV_{PP} (1.9 LSB) of output noise contribution due to the op amp alone, compared to about 594 μV_{PP} (less than 0.5 LSB) when that op amp is replaced with the LMP2015 which has no 1/f contribution. If the measurement time is increased from 100 seconds to 1 hour, the improvement realized by using the LMP2015 would be a factor of about 4.8 times (2.86 mV_{PP} compared to 596 µV when LMP2015 is used). This is mainly because the LMP2015 accuracy is not compromised by increasing the observation time.

D) Copper leadframe construction minimizes any thermocouple effects which would degrade low level/high gain data conversion application accuracy (see discussion in *"The Benefits of the LMP2015"* section).

E) Rail-to-Rail output swing maximizes the ADC dynamic range in 5V single supply converter applications. *Figure 7*and *Figure 8* are typical block diagrams showing the LMP2015 used as an ADC driver.

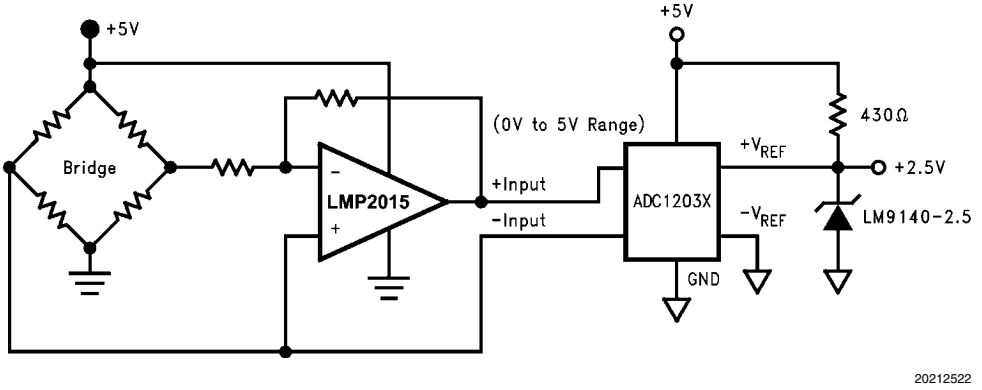
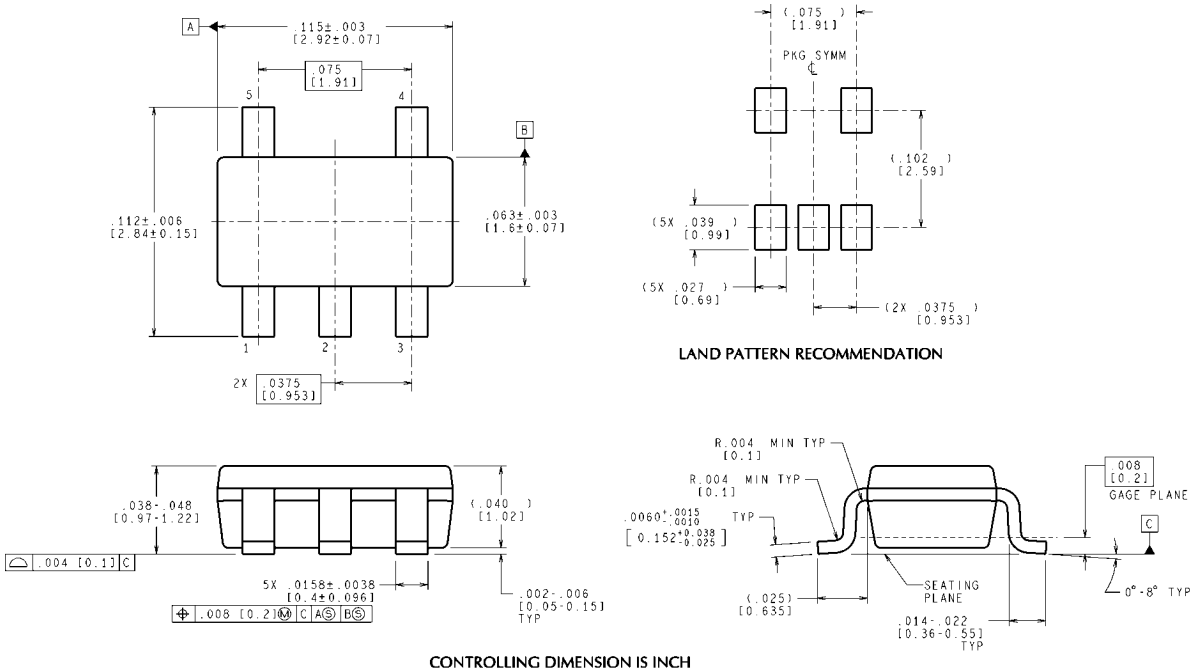
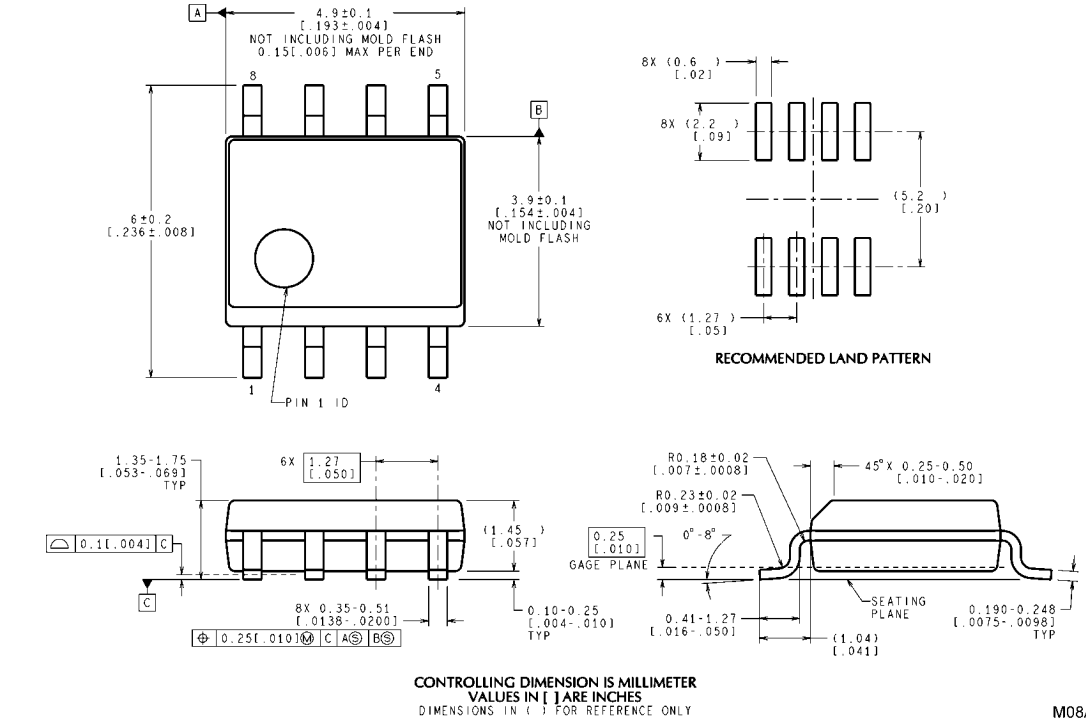


FIGURE 8. DC Coupled ADC Driver

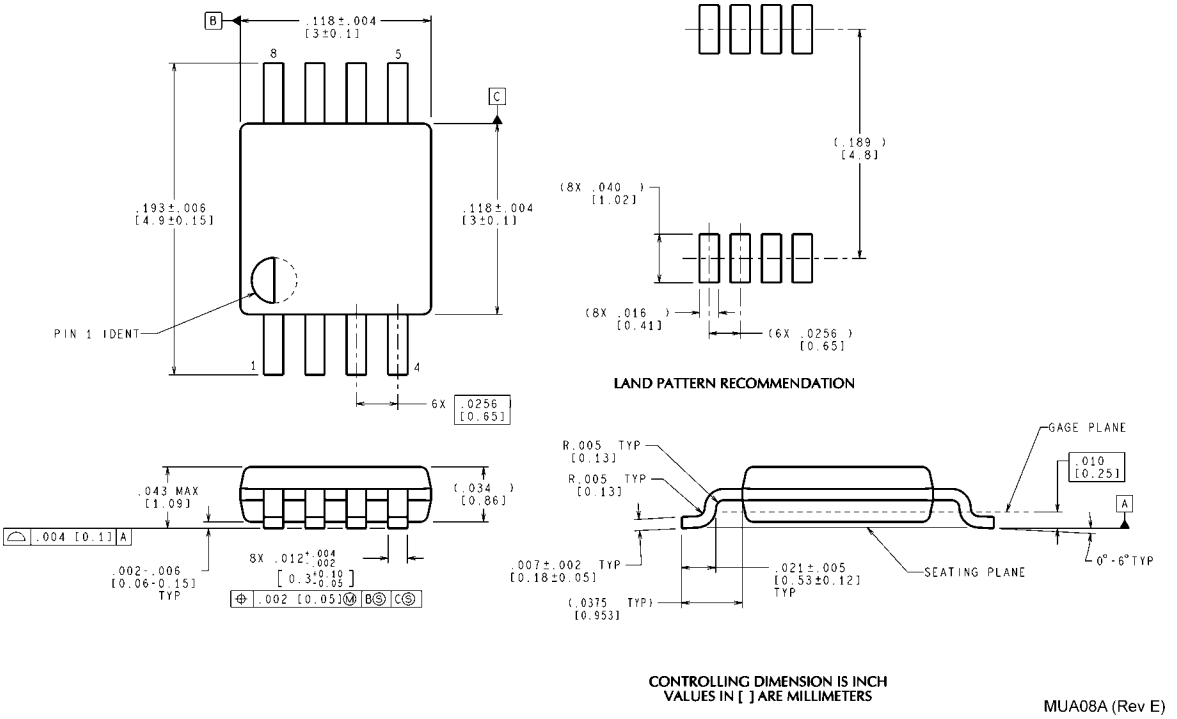
Physical Dimensions inches (millimeters) unless otherwise noted



5-Pin SOT23
NS Package Number MF0A5



8-Pin SOIC
NS Package Number M08A



8-Pin MSOP
NS Package Number MUA08A

Notes

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